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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,711	07/14/2003	Jason Cheng	M-9559-2P US	7093

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Jon W. Hallman
MacPHERSON KWOK CHEN & HEID LLP
Suite 226
1762 Technology Drive
San Jose, CA 95110

EXAMINER	
CHO, JAMES HYONCHOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,711	CHENG ET AL.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,8-12 and 14* is/are rejected.

7)☒ Claim(s) *2-7 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ~~7-14-2003~~ 12-12-03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt is acknowledged of the Amendment filed October 11, 2004.

Specification

The disclosure is objected to because of the following informalities: on page 1 of the specification, the expression, --now Patent No. 6,765,408-- should follow the filing date of parent application as recited on line 10.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 8-12 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by New et al. (US PAT No. 6,396,302).

Regarding claim 1, Fig. 9 of New et al. teaches a programmable logic device, comprising; a routing structure (routing signals to PL) configured to provide logical inputs; a plurality of logic blocks (SLICE0,... SLICE (m-1)), each logic block including a programmable AND array (PL) operable to provide a plurality of product terms (output of PL) from a plurality of the logical inputs provided by the routing structure, the plurality of product terms being arranged the same for each logic block (PL in SLICE1 ... SLICE

(m-1)); wherein a first one of the logic blocks forms a receiver logic block (SLICE 9m-1)) and a second one of the logic blocks forms a feeder logic block (SLICE0), the receiver logic block having an AND gate (AND gate in hXpGB, hXpGA, hXpFB, hXpFA) for each product term, each AND gate being operable to receive its product term and the corresponding product term in the feeder logic block (AND gate receives two inputs), each corresponding product term being cascaded from the feeder logic block over a dedicated lead (product term from SLICE0 hXpGB is fed to hXpGB of SLICE (m-1)).

Regarding, claim 8, Fig. 9 of New et al. teaches a programmable logic device, comprising: a routing structure (routing signals to PL) configured to provide logical inputs; a plurality of logic blocks (SLICE0,... SLICE (m-1)), arranged from a first logic block (SLICE0) to a last logic block (SLICE (m-1)) , wherein each logic block includes a programmable AND array (PL) operable to provide a plurality of product terms from a plurality of the logical inputs provided by the routing structure, the plurality of product terms being arranged the same for each logic block (PL in SLICE1 ... SLICE (m-1)), the first logic block being configured to cascade its products terms to the second logic block, the second logic block being configured to form the product of its product terms with the cascaded product terms from the first logic block and cascade the products to the third logic block, and so on such that the last logic block is configured to form the product of its product terms with the cascaded products from the next-to-the last logic block (SLICE0 to SLICE (m-1) are cascaded where the last SLICE (m-1) produces product term)., and wherein the cascaded product terms and products propagate

dedicated paths separate from the routing structure (routing structure for PL and path of product terms connecting hXpGB... hXpFA are separate)

Regarding claim 9, Fig. 9 of New et al. teaches the programmable logic device of claim 8 where each logic block is configured to form products of its product terms using logic circuitry (AND gate in hXpGB, hXpGA, hXpFB, hXpFA).

Regarding claim 10, Fig. 9 of New et al. teaches the programmable logic device of claim 9 where the logic circuitry comprises an AND gate for each product term (AND gate in hXpGB, hXpGA, hXpFB, hXpFA).

Regarding claim 11, Fig. 9 of New et al. teaches the programmable logic device of claim 8 where last logic block is a fourth logic block (when m=4, m-1 = 3 which is the fourth SLICE3).

Regarding claim 12, Fig. 9 of New et al. teaches a programmable logic device, comprising: a plurality of logic blocks (SLICE0,... SLICE (m-1)), each operable to provide a plurality of product terms (output of PL) selected from a plurality of logical inputs (g0 - g7, f0 - f7) provided by a routing structure (VIM G, VIM F), wherein the plurality of product terms is arranged the same for each logic block (same arrangement in SLICE0 and SLICE (m-1)) and wherein the size of the plurality of logical inputs is the same for each logic block (g0 - g7, f0 - f7, 16 inputs); and means for cascading product

terms, wherein the means is configured to form the product of the product terms from a first one of the logic blocks with the corresponding product terms selected from one or more of the remaining logic blocks, and wherein for each logic block selected, the maximum-achievable input width for the product is increased by the plurality of logical inputs (col. 16, line 43 - col. 17, line 64).

Regarding claim 14, Fig. 9 of New et al. teaches the programmable logic device of claim 12, wherein the plurality of logic blocks comprises four logic blocks (when m=4, m-1 = 3 which is the fourth SLICE3).

Allowable Subject Matter

Claims 2-7 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Although New et al. teaches a configurable logic element with expander structures, one of ordinary skill in the art would not have been motivated to modify the teaching of New et al. to further includes, among other things, the specific of each AND gate operable to receive its product term and the corresponding product term in the feeder logic block through the operation of programmable fuses, each logic block further comprising a plurality of macrocells, each macrocell coupling to a cluster OR gate operable to sum a cluster of the cascaded product terms from the AND gates such that

each macrocell may register the sum of cascaded product terms from its cluster OR gate, and the plurality of logical inputs being 68 inputs.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Veytsman et al. US PAT No. 5,969,539) discloses product term exporting mechanism.

Birkner et al. (US PAT No. 4,758,746) discloses a programmable logic array with added array of gates and added output routing flexibility.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819

October 14, 2004